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# 1 [System partitioning and timing analysis: HW/SW partitioning and code generation of embedded control applications on a reconfigurable architecture platform](#)



Massimo Baleani, Frank Gennari, Yunjian Jiang, Yatish Patel, Robert K. Brayton, Alberto Sangiovanni-Vincentelli

 May 2002 **Proceedings of the tenth international symposium on Hardware/software codesign**

Publisher: ACM Press

Full text available: pdf(575.30 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper studies the use of a reconfigurable architecture platform for embedded control applications aimed at improving real time performance. The hw/sw codesign methodology from POLIS is used. It starts from high-level specifications, optimizes an intermediate model of computation (Extended Finite State Machines) and derives both hardware and software, based on performance constraints. We study a particular architecture platform, which consists of a general purpose processor core, augmented w ...

**Keywords:** CSoc, code generation, hw/sw co-design

# 2 [Reconfigurable computing: architectures and applications: Application-specific instruction generation for configurable processor architectures](#)



Jason Cong, Yiping Fan, Guoling Han, Zhiru Zhang

 February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(253.53 KB)

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Designing an application-specific embedded system in nanometer technologies has become more difficult than ever due to the rapid increase in design complexity and manufacturing cost. Efficiency and flexibility must be carefully balanced to meet different application requirements. The recently emerged configurable and extensible processor architectures offer a favorable tradeoff between efficiency and flexibility, and a promising way to minimize certain important metrics (e.g., execution time, co ...

**Keywords:** ASIP, binate covering, compilation, configurable processor, technology mapping

### 3 Synthesis, Verification and Test: FPGA test time reduction through a novel

#### interconnect testing scheme

Stuart McCracken, Zeljko Zilic

February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

**Publisher:** ACM Press

Full text available:  pdf(675.59 KB) Additional Information: [full citation](#), [abstract](#), [references](#)

As device densities increase, testing cost is becoming a larger portion of the overall FPGA manufacturing cost. We present an approach to speed up testing FPGA interconnect by reconfiguring it during the test. Simple additions are made to create feedback shift register structures, which considerably reduce the number of test configurations for the switching matrix interconnect. This new testing architecture reduces switching matrix test time by 66% and the diagnosis time by 72%. The additions are ...

### 4 A coarse-grained FPGA architecture for high-performance FIR filtering

#### James R. Anderson, Siddharth Sheth, Kaushik Roy

March 1998 **Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays**

**Publisher:** ACM Press

Full text available:  pdf(1.21 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper introduces a coarse-grained FPGA architecture that is specialized for high-performance Finite Impulse Response (FIR) filtering. The proposed architecture provides the flexibility of a DSP processor with performance and area efficiency similar to that of a custom ASIC design, while allowing all of the basic FIR design parameters, including coefficient precision, to be configured. Previous research has already shown that FPGAs can provide a high-performance alternative to DSP processing ...

**Keywords:** architecture, digital signal processing, field programmable gate array, finite impulse response filtering

### 5 Cellular and Cryptographic Applications: Application of FPGA technology to accelerate the finite-difference time-domain (FDTD) method

#### Ryan N. Schneider, Laurence E. Turner, Michal M. Okoniewski

February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

**Publisher:** ACM Press

Full text available:  pdf(463.90 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)


The continuing advances in the field of electrical engineering, in areas like cellular communications, fiber optics, mobile and multi-gigahertz electronics have necessitated a computer-assisted design approach to the complex electromagnetic interactions and problems that arise. Finite-Difference Time-Domain (FDTD) Analysis is a very powerful tool for the modeling of electromagnetic phenomena. The algorithm is computationally intensive and simulations can run for a few hours to several days. Increasing ...

### 6 Whirlpool PLAs: a regular logic structure and their synthesis

#### Fan Mo, Robert K. Brayton

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

**Publisher:** ACM Press

Full text available:  pdf(213.57 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

A regular circuit structure called a Whirlpool PLA (WPLA) is proposed. It is suitable for the implementation of finite state machines as well as combinational logic. A WPLA is logically a four-level Boolean NOR network. By arranging the four logic arrays in a cycle, a compact layout is achieved. Doppio-ESPRESSO, a four-level logic minimization algorithm is developed for WPLA synthesis. No technology mapping, placement or routing is necessary for the WPLA. Area and delay trade-off is absent, beca ...

## 7 Optimized implementations of the multi-configuration DFT technique for analog circuits

M. Renovell, F. Azaïs, Y. Bertrand

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

**Publisher:** IEEE Computer Society

Full text available:  pdf(109.68 KB)



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Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The paper describes an approach to optimize the application of the multi-configuration DFT technique for analog circuits. This technique allows to emulate the circuit in a number of new test configurations targeting the maximum fault coverage. The brute force application of the multi-configuration is shown to produce a very significant improvement of the original poor testability. An optimized approach is proposed to apply this DFT technique in a more refined way. The optimization problem consis ...

**Keywords:** VLSI, Analog Circuit, Mixed Signal Circuit, Test.

## 8 Novel devices and approaches to programmable devices: Nanowire-based sublithographic programmable logic arrays



Andre DeHon, Michael J. Wilson

February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

**Publisher:** ACM Press

Full text available:  pdf(718.33 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#), [review](#)

How can Programmable Logic Arrays (PLAs) be built without relying on lithography to pattern their smallest features? In this paper, we detail designs which exploit emerging, bottom-up material synthesis techniques to build PLAs using molecular-scale nanowires. Our new designs accommodate technologies where the only post-fabrication programmable element is a non-restoring diode. We introduce stochastic techniques which allow us to restore the diode logic at the nanoscale so that it can be cascade ...


**Keywords:** nanowires, programmable logic arrays, sublithographic architecture

## 9 Spare allocation and reconfiguration in large area VLSI

Sy-Yen Kuo, W. Kent Fuchs

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**

**Publisher:** IEEE Computer Society Press

Full text available:  pdf(491.53 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

One approach to enhancing the yield of large area VLSI is through design for yield enhancement by means of restructurable interconnect, logic and computational elements. Although extensive literature exists concerning architectural design for inclusion of spares and restructuring mechanisms in memories and processor arrays, little research has been published on optimal spare allocation and reconfiguration in the presence of multiple


defects. In this paper, a summary of a systematic approach ...

10 Interactive design language: A unified approach to hardware simulation, synthesis and documentation

L. I. Maissel, D. L. Ostapko

January 1982 **Proceedings of the 19th conference on Design automation**

**Publisher:** IEEE Press

Full text available:  [pdf\(797.73 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

IDL is a hardware design language in use in the VLSI environment. It incorporates a significant number of high-level features such as groups, subroutines, and labels and is particularly well adapted to dealing with parallelism at the hardware level. In addition to being human intelligible (and therefore appropriate as a documentation medium), IDL code can be used to generate 2-level logic which, under the IDL system, can be manipulated in a number of ways, including product term factoring a ...

11 Arithmetic: A faster distributed arithmetic architecture for FPGAs



Radhika S. Grover, Weijia Shang, Qiang Li

February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

**Publisher:** ACM Press

Full text available:  [pdf\(379.35 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#)

Distributed Arithmetic (DA) is an important technique to implement digital signal processing (DSP) functions in FPGAs. However, traditional lookup table (LUT) based DA architectures contain one or more carry propagation chains in the critical path that dictates the fastest time at which an entire design can run. In this paper, we describe a novel technique that can reduce or eliminate the carry-propagate chain from the critical path in LUT based DA architectures on FPGAs. In the proposed scheme, ...

**Keywords:** DALUT, XC4000, carry propagation, cost-performance analysis, distributed arithmetic

12 A concept for test and reconfiguration of a fault-tolerant VLSI processor system



K. E. Grosspietsch, J. Kaiser, E. Nett

May 1980 **Proceedings of the 7th annual symposium on Computer Architecture**

**Publisher:** ACM Press

Full text available:  [pdf\(514.61 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The following paper is to present a test and reconfiguration strategy for fault-tolerant VLSI processor systems. This is accomplished with respect to the requirements imposed by the VLSI technology. The proposed concept is exemplified by a model composed of four microprogrammable processors each with a local memory. The test strategy of a gradually expanding hardcore is applied where the central hardcore consists of a small test unit of low complexity. This test unit enables each processor ...

13 Automated design of finite state machine predictors for customized processors



Timothy Sherwood, Brad Calder

May 2001 **ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture ISCA '01**, Volume 29 Issue 2

**Publisher:** ACM Press

Full text available:  [pdf\(914.12 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

*Customized processors use compiler analysis and design automation techniques to take a generalized architectural model and create a specific instance of it which is optimized to a given application or set of applications. These processors offer the promise of satisfying the high performance needs of the embedded community while simultaneously shrinking design times.*

*Finite State Machines (FSM) are a fundamental building block in computer architecture, and are used to control ...*

#### 14 Programming environments for highly parallel multiprocessors



A. P. Reeves

January 1988

**Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1**

**Publisher:** ACM Press

Full text available: pdf(1.07 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Emerging highly parallel multiprocessors offer an exciting alternative to conventional pipelined supercomputers for a variety of computationally intensive scientific applications. A factor that has impeded the introduction of these multiprocessor systems is that conventional languages, such as Fortran, cannot be directly used and new programming techniques must be mastered. A key issue for highly parallel systems is the development of appropriate programming environments. Program ...

#### 15 Arctic: A functional language for real-time control



Roger B. Dannenberg

August 1984

**Proceedings of the 1984 ACM Symposium on LISP and functional programming**

**Publisher:** ACM Press

Full text available: pdf(631.26 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Arctic is a language for the specification and implementation of real-time control systems. Unlike more conventional languages for real-time control, which emphasize concurrency, Arctic is a stateless language in which the relationships between system inputs, outputs and intermediate terms are expressed as operations on time-varying functions. Arctic allows discrete events or conditions to invoke and modify responses asynchronously, but because programs have no state, synchronization problem ...

#### 16 Tools: Low-power technology mapping for FPGA architectures with dual supply voltages



Deming Chen, Jason Cong, Fei Li, Lei He

February 2004

**Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

**Publisher:** ACM Press

Full text available: pdf(313.18 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper we study the technology mapping problem of FPGA architectures with dual supply voltages (Vdds) for power optimization. This is done with the guarantee that the mapping depth of the circuit will not increase compared to the circuit with a single Vdd. We first design a single-Vdd mapping algorithm that achieves better power results than the latest published low-power mapping algorithms. We then show that our dual-Vdd mapping algorithm can further improve power savings by up to 11.6% ...

**Keywords:** dual supply voltage, low-power FPGA, technology mapping

17 Ultracomputers

Jacob T. Schwartz

October 1980 **ACM Transactions on Programming Languages and Systems (TOPLAS)**,  
Volume 2 Issue 4**Publisher:** ACM Press

Full text available: pdf(2.54 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

A class of parallel processors potentially involving thousands of individual processing elements is described. The architecture is based on the perfect shuffle connection and has two favorable characteristics: (1) Each processor communicates with a fixed number of other processors. (2) Important communication functions can be accomplished in time proportional to the logarithm of the number of processors. A number of basic algorithms for these "ultracomputers" are presented, and ...

18 A new method to express functional permissibilities for LUT based FPGAs and its applications

Shigeru Yamashita, Hiroshi Sawada, Akira Nagoya

January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design****Publisher:** IEEE Computer Society

Full text available: pdf(488.91 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)[Publisher Site](#)

This paper presents a new method to express functional permissibilities for look-up table (LUT) based field programmable gate arrays (FPGAs). The method represents functional permissibilities by using sets of pairs of functions, not by incompletely specified functions. It makes good use of the properties of LUTs such that their internal logics can be freely changed. The permissibilities expressed by the proposed method have the desired property that at many points of a network they can be simultaneous ...

**Keywords:** FPGA, look-up table (LUT), functional permissibility, optimization, routing

19 VLSI in the nanometer era: Exploiting multiple functionality for nano-scale reconfigurable systems

Paul Beckett

April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI****Publisher:** ACM Press

Full text available: pdf(197.22 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

It is likely that it will become increasingly difficult to manufacture the complex, heterogeneous logic structures that characterise current reconfigurable logic systems. As a result, these systems may come to be characterised by vast arrays of largely identical devices that are differentiated via post-fabrication configuration - but only if low-overhead configuration can be achieved. Two simulation studies are presented that describe some ideas for achieving low-overhead reconfigurability in systems ...

**Keywords:** RTD, carbon nanotube, chalcogenide, double gate transistors, multi-valued RAM, multiple functionality, nanoelectronics, nanotechnology, reconfigurable systems, resonant tunneling

## 20

On finding non-intersecting paths in grids and its application in reconfiguring

VLSI/WSI arrays

Vwani P. Roychowdhury, Jehoshua Bruck

January 1990 **Proceedings of the first annual ACM-SIAM symposium on Discrete algorithms****Publisher:** Society for Industrial and Applied MathematicsFull text available:  pdf(984.92 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

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Proceedings of the IEEE **VLSI** Signal Processing Workshop, San Francisco, October 1996.

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IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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## 1. Design of RM-nc: a reconfigurable neurocomputer for massively parallel-computations

Erdogan, S.S.; Wahab, A.;  
Neural Networks, 1992. IJCNN., International Joint Conference on  
Volume 2, 7-11 June 1992 Page(s):33 - 38 vol.2  
Digital Object Identifier 10.1109/IJCNN.1992.226988

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## 2. VHDL modeling and simulation of the back-propagation algorithm and its RM

Erdogan, S.S.; Wahab, A.; Hong, T.H.;  
Custom Integrated Circuits Conference, 1993., Proceedings of the IEEE 1993  
9-12 May 1993 Page(s):3.3.1 - 3.3.4  
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